

## IN THE CLAIMS

What is claimed is:

1. 1. A method comprising:
  2. providing a substrate comprising a first transistor structure comprising an n-type gate material and second transistor structure comprising an p-type gate material;
  5. selectively removing the n-type gate material to form a recess in the first gate structure; and
  7. filling the recess with an n-type metal gate material.
1. 2. The method of claim 1 wherein providing a substrate comprising a first transistor structure comprising an n-type gate material and second transistor structure comprising a p-type gate material comprises providing a substrate comprising an NMOS transistor structure comprising an n doped polysilicon gate material and a PMOS transistor structure comprising a p doped polysilicon gate material.
1. 3. The method of claim 2 wherein providing a substrate comprising an NMOS transistor structure comprising an n doped polysilicon gate material and an PMOS transistor structure comprising a p doped polysilicon gate material comprises providing a substrate comprising an NMOS transistor

5 structure comprising an n doped polysilicon gate material and a PMOS  
6 transistor structure comprising a p doped polysilicon gate, wherein the PMOS  
7 transistor structure comprises source and drain regions comprising a silicon  
8 germanium alloy.

1 4. The method of claim 1 wherein selectively removing the n-type gate  
2 material comprises selectively removing the n-type gate material by wet  
3 etching the n-type gate material with a mixture of about 2 percent to about 30  
4 percent ammonium hydroxide in deionized water and applying a sonication  
5 from about 0.5 MHz to about 1.2 MHz.

1 5. The method of claim 4 wherein wet etching the n-type gate material  
2 with a mixture of about 10 percent to about 20 percent ammonium hydroxide  
3 in deionized water comprises wet etching the n-type gate material with a  
4 mixture of about 10 percent to about 20 percent ammonium hydroxide in  
5 deionized water at a temperature from about 10 degrees to about 40 degrees  
6 Celsius.

1 6. The method of claim 1 wherein selectively removing the n-type gate  
2 material comprises wet etching the n-type gate material with a mixture of  
3 about 15 percent to about 30 percent tetramethylammonium hydroxide in

4 deionized water and applying a sonication from about 0.8 MHz to about 1.2  
5 MHz.

1 7. The method of claim 6 wherein wet etching the n-type gate material  
2 with a mixture of about 15 percent to about 30 percent tetramethylammonium  
3 hydroxide in deionized water comprises wet etching the n-type gate material  
4 with a mixture of about 15 percent to about 30 percent tetramethylammonium  
5 hydroxide in deionized water at a temperature from about 60 degrees to  
6 about 90 degrees Celsius.

1 8. The method of claim 1 wherein selectively removing the n-type gate  
2 material comprises selectively removing the n-type gate material and not  
3 substantially removing the p-type gate material.

1 9. The method of claim 1 wherein selectively removing the n-type gate  
2 material to form a recess in the first gate structure further comprises  
3 selectively removing a first gate dielectric layer disposed beneath the n-type  
4 gate material.

1 10. The method of claim 9 wherein selectively removing the first gate  
2 dielectric layer disposed beneath the n-type gate material further comprises  
3 forming a second gate dielectric layer within the recess.

1       11. The method of claim 10 wherein forming the second gate dielectric  
2       layer within the recess comprises forming a high k gate dielectric layer within  
3       the recess.

1       12. The method of claim 10 wherein selectively removing a first gate  
2       dielectric layer disposed beneath the n-type gate material further comprises  
3       forming a high k gate dielectric layer selected from the group consisting of  
4       hafnium oxide, zirconium oxide, titanium oxide, and aluminum oxide and /or  
5       combinations thereof within the recess.

1       13. The method of claim 1 wherein filling the recess with an n-type metal  
2       gate material comprises filling the recess with a metal gate material selected  
3       from the group consisting of hafnium, zirconium, titanium, tantalum, and  
4       aluminum and /or combinations thereof.

1       14. A method of forming a microelectronic structure comprising;  
2               providing a substrate comprising an n-type transistor structure  
3       comprising an n-type polysilicon gate material and a p-type transistor  
4       structure comprising a p-type polysilicon gate material, wherein a first  
5       dielectric layer is disposed above the n-type and the p-type gate structures;  
6               removing a portion of the first dielectric layer so that the n-type  
7       polysilicon gate material is exposed;

8                   selectively removing the n-type polysilicon gate material to form a  
9                   recess; and  
10                  filling the recess with an n-type metal gate material.

1                  15.    The method of claim 14 wherein filling the recess with an n- type  
2                  metal gate material further comprises forming a second dielectric layer on the  
3                  n-type metal gate material.

1                  16.    The method of claim 14 wherein selectively removing the n-type  
2                  polysilicon gate material comprises selectively removing the n-type  
3                  polysilicon gate material and not substantially removing the p-type polysilicon  
4                  gate material.

1                  17.    The method of claim 14 wherein selectively removing the n-type  
2                  polysilicon gate material comprises selectively removing the n-type gate  
3                  material by wet etching the n-type gate material with a mixture of about 2  
4                  percent to about 30 percent ammonium hydroxide in deionized water and  
5                  applying a sonication from about 0.5 MHz to about 1.2 MHz.

1                  18.    A structure comprising:  
2                  a substrate comprising an n-type transistor structure comprising an n-

3 type metal gate material and a p-type transistor structure comprising a p-type  
4 polysilicon gate material.

5 19. The structure of claim 18 wherein the p-type transistor structure  
6 further comprises a source and a drain region comprising a silicon  
7 germanium alloy.

1 20. The structure of claim 18 wherein the n-type transistor structure  
2 further comprises a high k gate dielectric layer selected from the group  
3 consisting of hafnium oxide, zirconium oxide, titanium oxide, and aluminum  
4 oxide and /or combinations thereof.

1 21. The structure of claim 18 wherein the n-type metal gate material is  
2 selected from the group consisting of hafnium, zirconium, titanium, tantalum  
3 and aluminum and /or combinations thereof.